AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A power factor correction circuit for correcting an input power factor by allowing a rectified voltage, obtained by rectifying an alternating current power-supply voltage of an alternating current power-supply with a rectifying circuit, to be inputted to a main switch via a booster reactor and allowing the main switch to be turned on or turned off while converting the power-supply voltage into a direct current output voltage, comprising:

a first series circuit connected between one output terminal and the other output terminal of the rectifying circuit and including a booster winding and a wind-up winding, both wound on the booster reactor, a first diode and a smoothing capacitor;

a second series circuit connected between the one output terminal and the other output terminal of the rectifying circuit and including the booster winding of the booster reactor, a zero-current switching reactor and the main switch;

a second diode connected between a junction, between the main switch and the zero-current switching reactor, and the smoothing capacitor; and

control means for controllably turning on and off the main switch to control an output voltage of the smoothing capacitor to a given voltage.

2. (Original) A power factor correction circuit for correcting an input power factor by allowing a rectified voltage, obtained by rectifying an alternating current power-supply voltage of an alternating current power-supply with a rectifying circuit, to be inputted to a

main switch via a booster reactor and allowing the main switch to be turned on or turned off while converting the power-supply voltage into a direct current output voltage, comprising:

a first series circuit connected between one output terminal and the other output terminal of the rectifying circuit and including a booster winding and a wind-up winding, both wound on the booster reactor, a zero-current switching reactor, a first diode and a smoothing capacitor;

a second series circuit connected between one output terminal and the other output terminal of the rectifying circuit and including the booster winding of the booster reactor, and the main switch;

a second diode connected between a junction, between the booster winding and the wind-up winding of the booster reactor, and the main switch and the smoothing capacitor; and

control means for controllably turning on and off the main switch to control an output voltage of the smoothing capacitor to a given voltage.

3. (Original) The power factor correction circuit according to claims 1 or 2, further comprising:

a third series circuit connected to the main switch in parallel and including a third diode and a snubber capacitor;

a fourth series circuit connected between a junction, between the third diode and the snubber capacitor, and one terminal of the first diode and including a fourth diode, a regenerative winding wound on the booster reactor, a current limiting reactor and a regenerative capacitor; and

a fifth diode connected between a junction, between the regenerative capacitor and the current limiting reactor, and a junction between the other terminal of the first diode and the smoothing capacitor.

4. (Currently amended) The power factor correction circuit according to ~~claims~~ claim ~~2 or~~ 3, wherein the zero-current switching reactor and the current limiting reactor include a leakage inductor between windings of the booster reactor.

5. (Original) The power factor correction circuit according to claim 4, wherein the booster reactor includes the wind-up winding and the regenerative winding that are wound on a core in a nondense-coupled condition with respect to the booster winding.

6. (Currently amended) The power factor correction circuit according to ~~claims~~ claim 4 ~~or 5~~, wherein the booster reactor is arranged to have a bypass root of a magnetic flux among the wind-up winding, the booster winding and the regenerative winding.

7. (Original) The power factor correction circuit according to claims 1 or 2, further comprising:

a third series circuit connected to the main switch in parallel and including a third diode and a snubber capacitor;

a fourth series circuit connected between a junction, between the third diode and the snubber capacitor, and one terminal of the first diode and including a fourth diode, a capacitor, and a regenerative capacitor; and

a fifth diode connected between a junction, between the regenerative capacitor and the capacitor, and a junction between the other terminal of the first diode and the smoothing capacitor.

8. (Currently amended) The power factor correction circuit according to ~~any one of~~ ~~claims~~ claim 3 ~~to 7~~, wherein the control means is operative to allow the main switch to execute zero-current switching when turned on and to execute zero voltage switching when turned off.

9. (Currently amended) The power factor correction circuit according to any one of claims 1 ~~to 8~~ or 2, wherein the control means controls a switching frequency of the main switch in dependence on a value of an alternating current power-supply voltage of the alternating current power-supply.

10. (Original) The power factor correction circuit according to claim 9, wherein the control means includes:

first error voltage generating means for amplifying an error between the output voltage and a reference voltage to generate a first error voltage signal;

multiplied output voltage generation means for multiplying the first error voltage signal of the first error voltage generating means and the rectified voltage of the rectifying circuit to generate a multiplied output voltage;

current detection means for detecting an input current flowing through the rectifying circuit;

second error voltage generation means for amplifying an error between a voltage depending on the input current, detected by the current detection means, and the multiplied output voltage of the multiplied output voltage generation means;

frequency control means for generating a frequency control signal, by which a switching frequency of the main switch is varied, depending on a value of the rectified voltage of the rectifying circuit; and

pulse width control means for controlling a pulse width depending on the second error voltage signal of the second error voltage generation means and generating a pulse signal, by which the switching frequency of the main switch is varied, in dependence on the frequency control signal generated by the frequency control means, to allow the pulse signal to be applied to the main switch for controlling the output voltage to the given voltage.

11. (Currently amended) The power factor correction circuit according to ~~claims~~ claim 9 ~~or 10~~, wherein the control means is operative to set the switching frequency to a lower limit frequency when the alternating current power-supply voltage is less than a lower limit preset voltage and set the switching frequency to an upper limit frequency when the alternating current power-supply voltage exceeds an upper limit preset voltage while varying the switching frequency from the lower limit frequency to the upper limit frequency under circumstances where the alternating current power-supply voltage remains in a range between the lower limit preset voltage and the upper limit preset voltage.

12. (Original) The power factor correction circuit according to claim 11, wherein the control means is operative to interrupt switching operations of the main switch under circumstances where the alternating current power-supply voltage is less than the lower limit preset voltage.

13. (Currently amended) The power factor correction circuit according to ~~any one of~~ claims 1 ~~to 12~~ or 2, further comprising:

a rush current limiting resistor connected between the rectifying circuit and the smoothing capacitor and decreasing a rush current of the smoothing capacitor when the alternating current power-supply is turned on; and

wherein the main switch includes a normally turned on type switch; and

the control means is operative to turn the main switch off in response to a voltage developed across the rush current limiting resistor when the alternating current power-supply is turned on and begins switching operations to turn on and off the main switch after the smoothing capacitor is charged.

14. (Original) The power factor correction circuit according to claim 13, wherein the booster reactor further includes an auxiliary winding and further comprising:

a normal operation power-supply section operative to supply a voltage developed across the auxiliary winding to the control means.

15. (Currently amended) The power factor correction circuit according to ~~claims~~ claim 13 ~~or 14~~, further comprising a semiconductor switch connected to the rush current limiting resistor in parallel, wherein the control means turns on the semiconductor switch after switching operations of the main switch are commenced.

16. (Original) The power factor correction circuit according to claim 1, further comprising:
a fifth series circuit including a first capacitor, and a sixth diode connected between a junction, between the wind-up winding of the booster reactor and the first diode, and the smoothing capacitor; and
a seventh diode connected between a junction, between the first capacitor and the sixth diode, and the smoothing capacitor.

17. (Original) The power factor correction circuit according to claim 2, further comprising:

a fifth series circuit including a first capacitor, and a sixth diode connected between a junction, between the zero-current switching reactor and the first diode, and the smoothing capacitor; and

a seventh diode connected between a junction, between the first capacitor and the sixth diode, and the smoothing capacitor.

18. (Original) The power factor correction circuit according to claims 1 or 2, wherein the booster reactor includes a core having first to third legs, in which a magnetic circuit is

formed, and wherein the first leg is wound with the booster winding and the second leg is wound with the wind-up winding whereas the third leg is used as a pass core.

19. (Original) The power factor correction circuit according to claim 3, wherein the booster reactor includes a core having first to third legs, in which a magnetic circuit is formed, and wherein the first leg is wound with the booster winding, the second leg is wound with the wind-up winding and the third leg is wound with the regenerative winding.

20. (Currently amended) The power factor correction circuit according to ~~claims~~ claim 18 ~~or 19~~, wherein the respective legs of the core have gaps with an equal thickness.

21. (Original) The power factor correction circuit according to claim 20, wherein each gap formed in the core is provided with a magnetic body that varies in permeability depending on a current flowing through each winding.

22. (Original) The power factor correction circuit according to claim 20, wherein each gap formed in the core is provided with a magnetic body, which varies in permeability depending on a current flowing through each winding, and an air gap.

23. (New) The power factor correction circuit according to claim 7, wherein the control means is operative to allow the main switch to execute zero-current switching when turned on and to execute zero voltage switching when turned off.

24. (New) The power factor correction circuit according to claim 19, wherein the respective legs of the core have gaps with an equal thickness.

25. (New) The power factor correction circuit according to claim 24, wherein each gap formed in the core is provided with a magnetic body that varies in permeability depending on a current flowing through each winding.

26. (New) The power factor correction circuit according to claim 24, wherein each gap formed in the core is provided with a magnetic body, which varies in permeability depending on a current flowing through each winding, and an air gap.

27. (New) The power factor correction circuit according to claim 5, wherein the booster reactor is arranged to have a bypass root of a magnetic flux among the wind-up winding, the booster winding and the regenerative winding.